

Figure 1 – Sensor Block Diagram

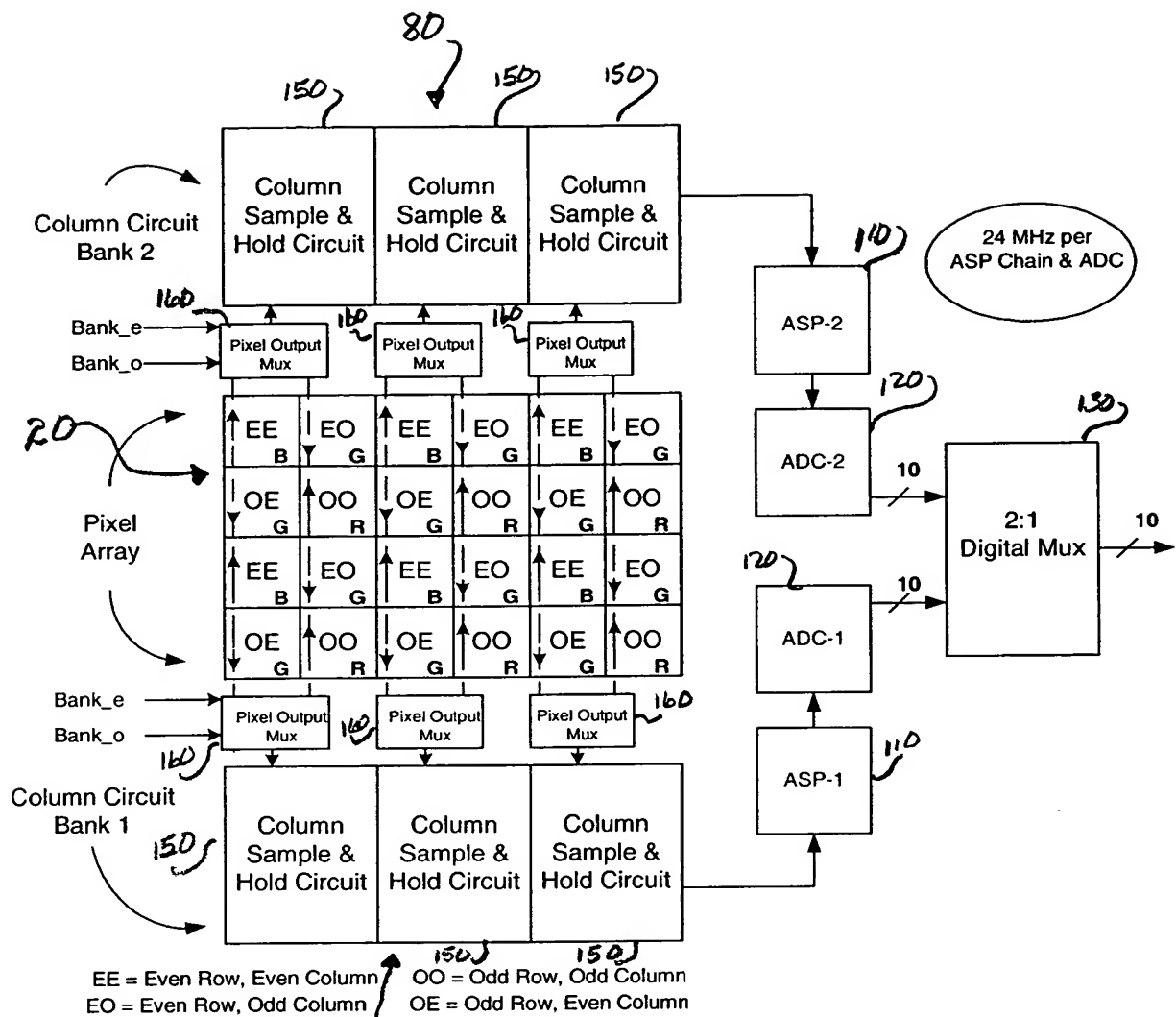


Figure 2 - Sensor Architecture Diagram

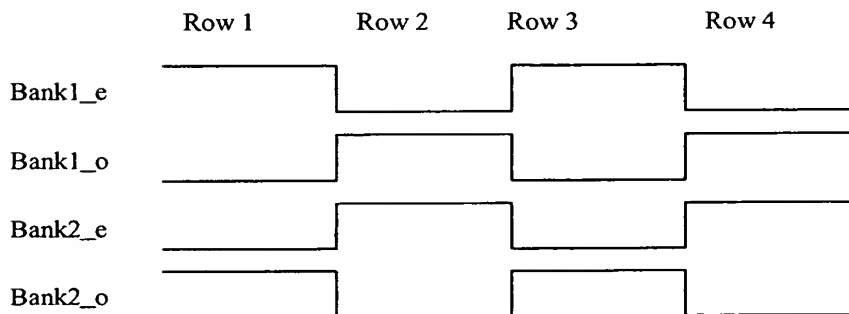
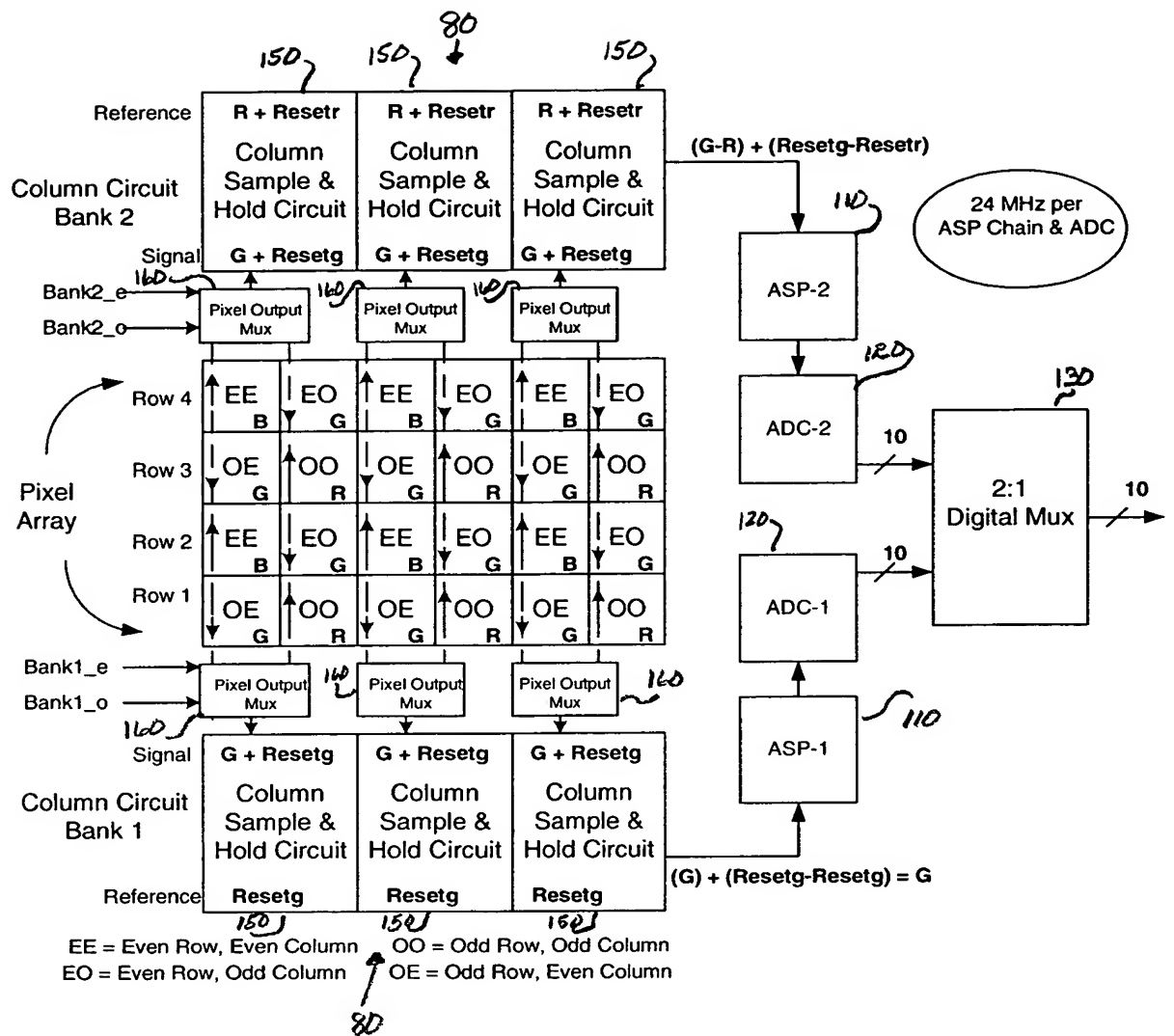


Figure 3 – Sensor Timing for Color Difference Readout

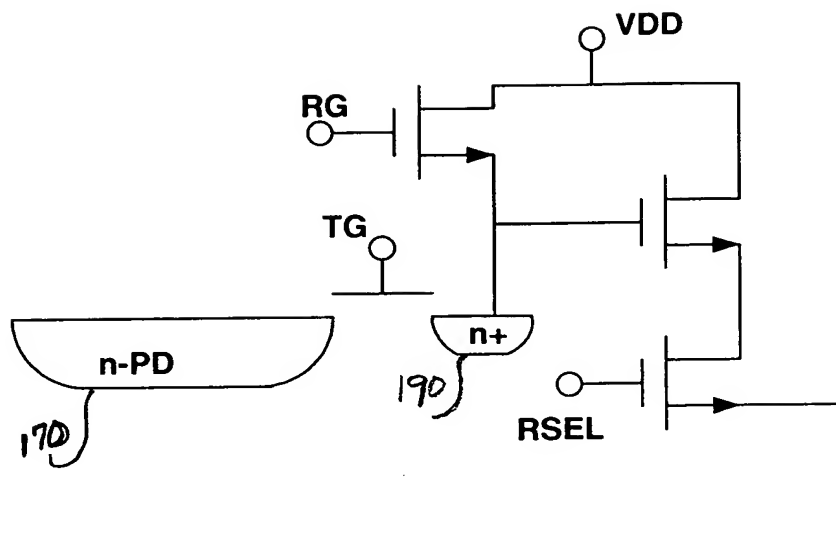


Figure 4 – 4 Transistor Pixel

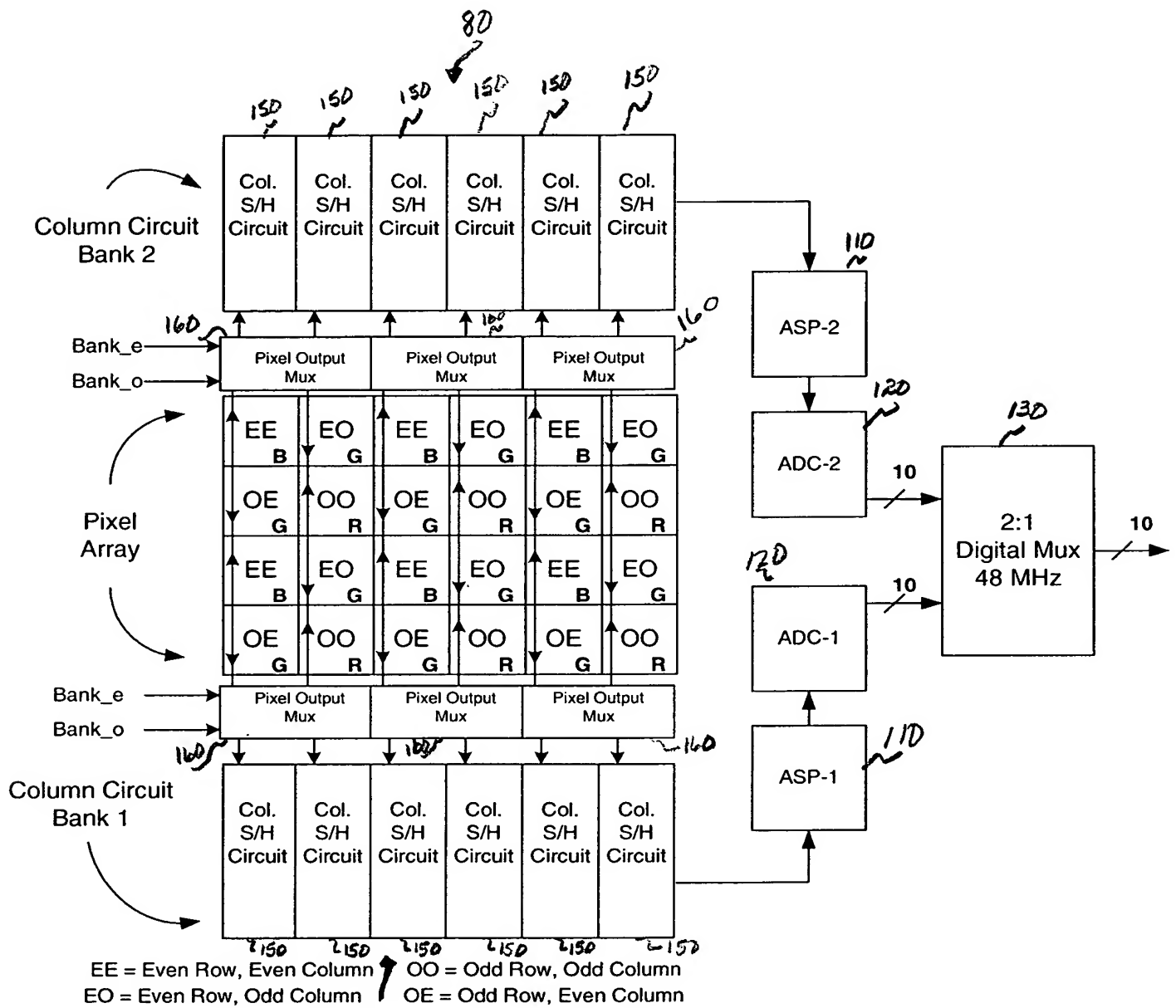


Figure 5a - Sensor Architecture Diagram

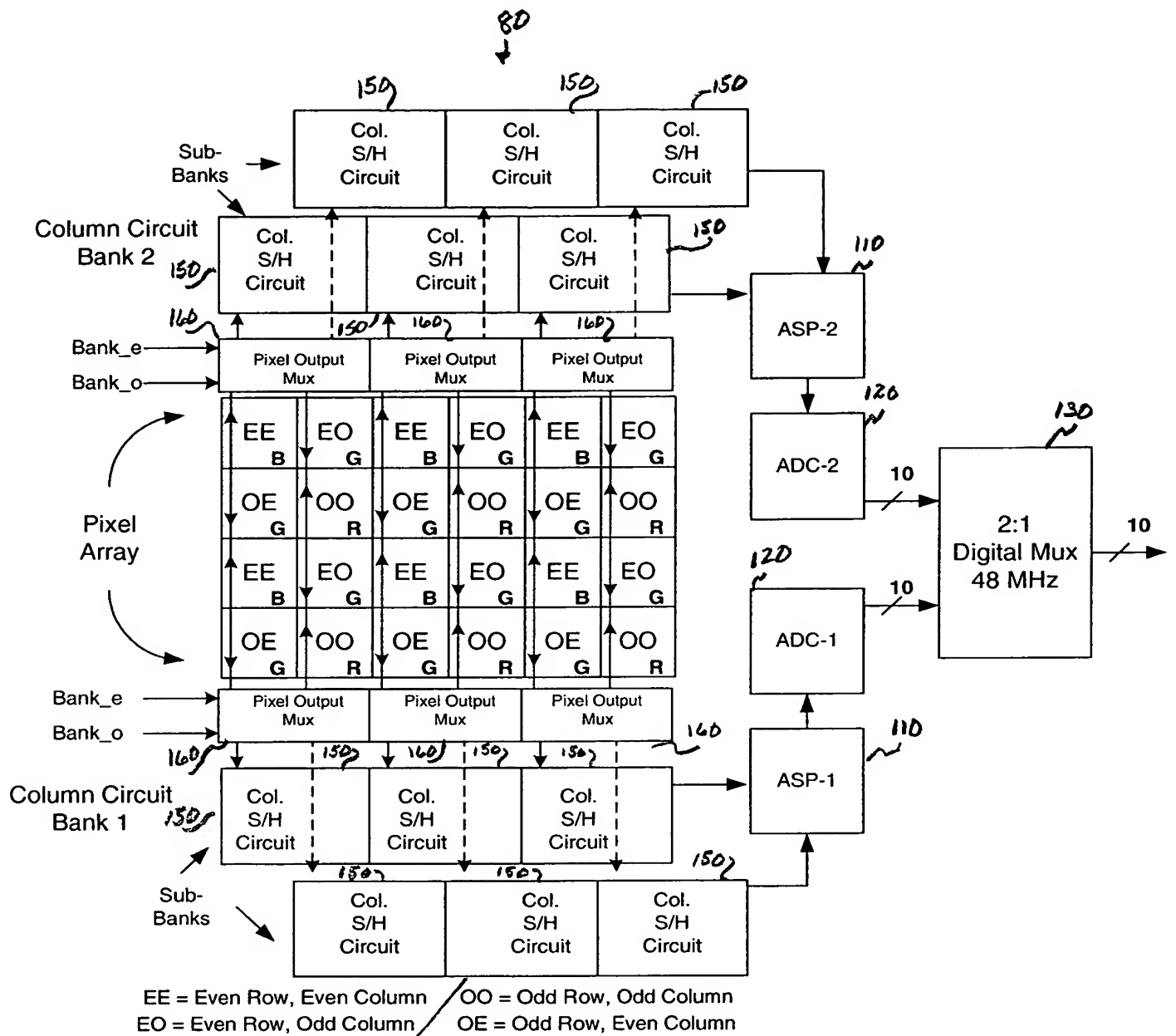


Figure 5b - Sensor Architecture Diagram

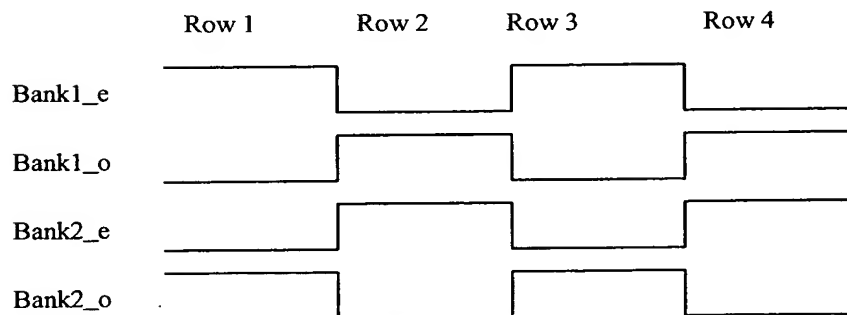
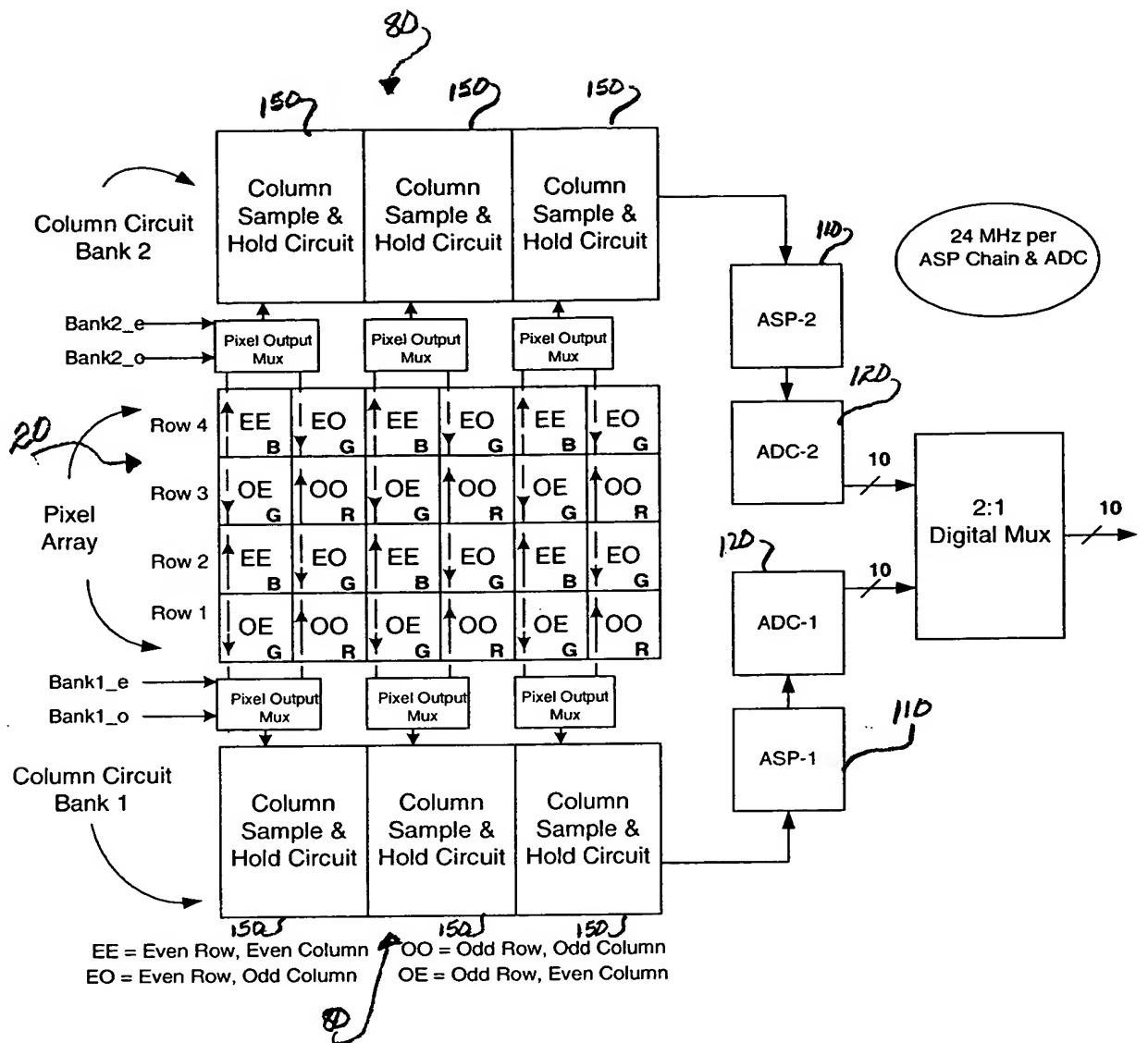


Figure 6a – Pixel Output Multiplexer Timing Diagram for Color Plane Separation

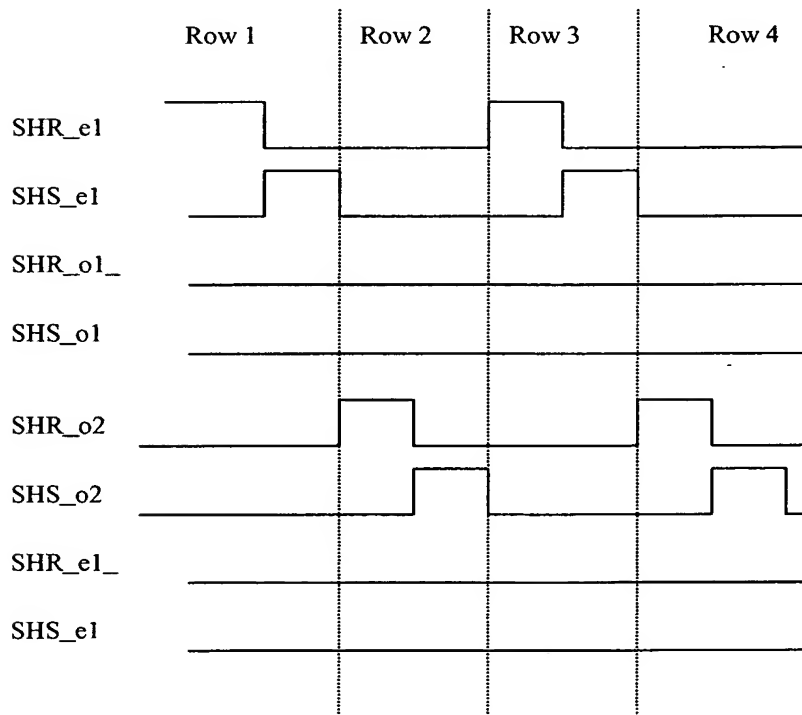
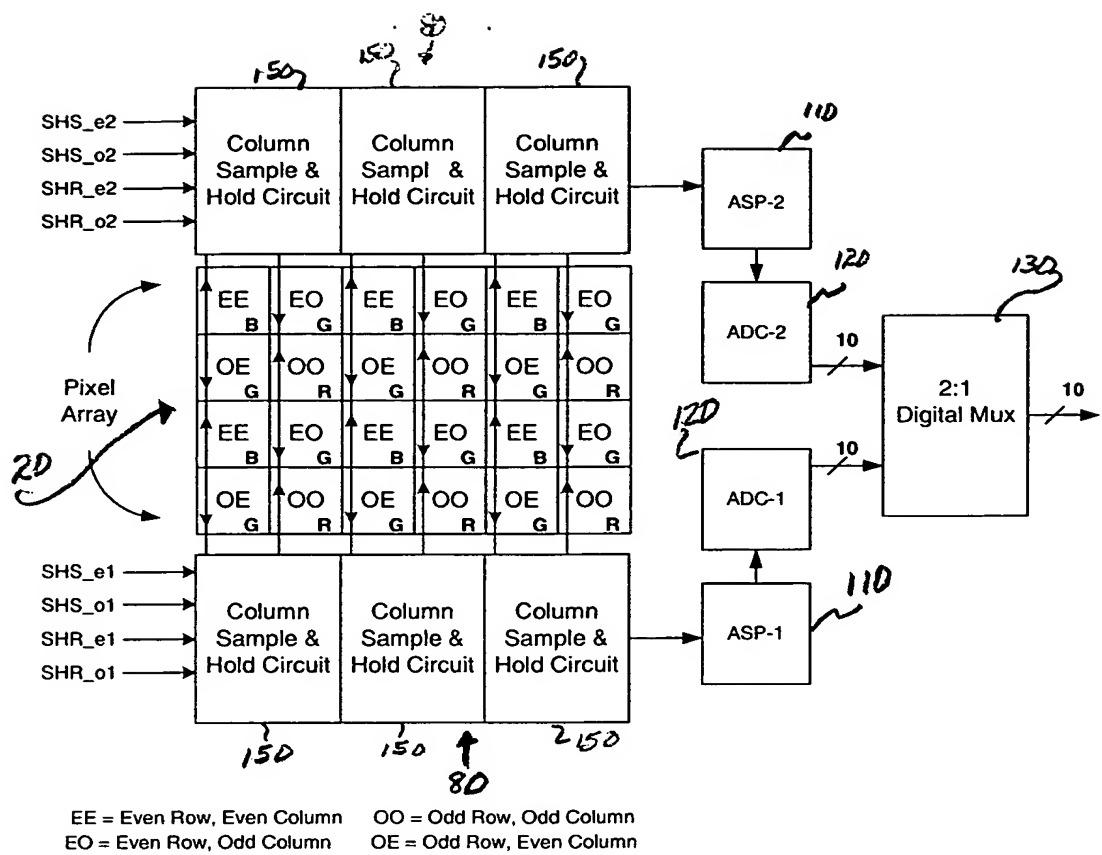


Figure 6b – Pixel Output Multiplexer Timing Diagram for Color Plane Separation

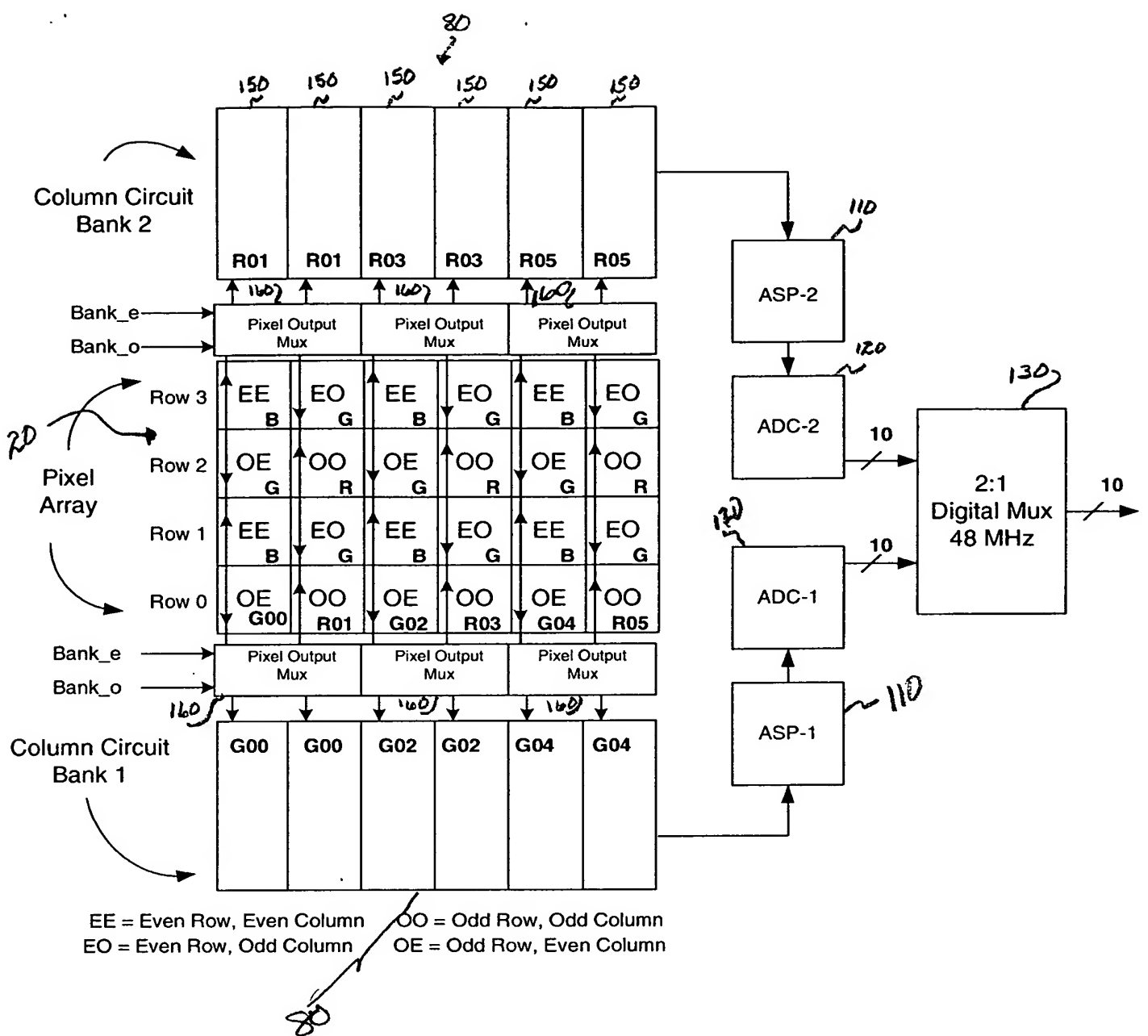


Figure 6c – Sensor Block Diagram for Adjacent Sample Averaging

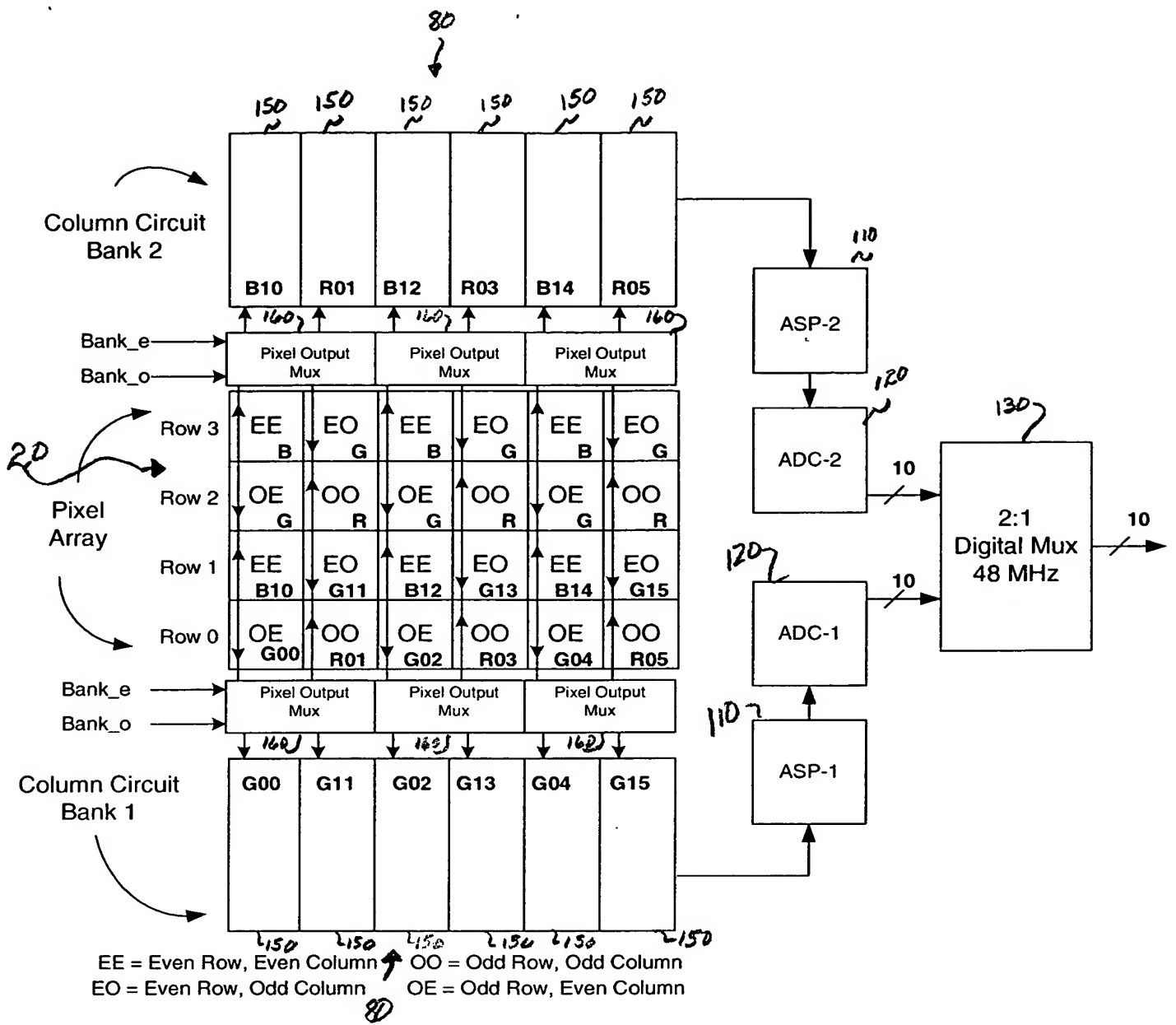


Figure 6d – Sensor Block Diagram for Adjacent Sample Averaging
Two Row Readout



Figure 7: 4-shared Pixel Schematic

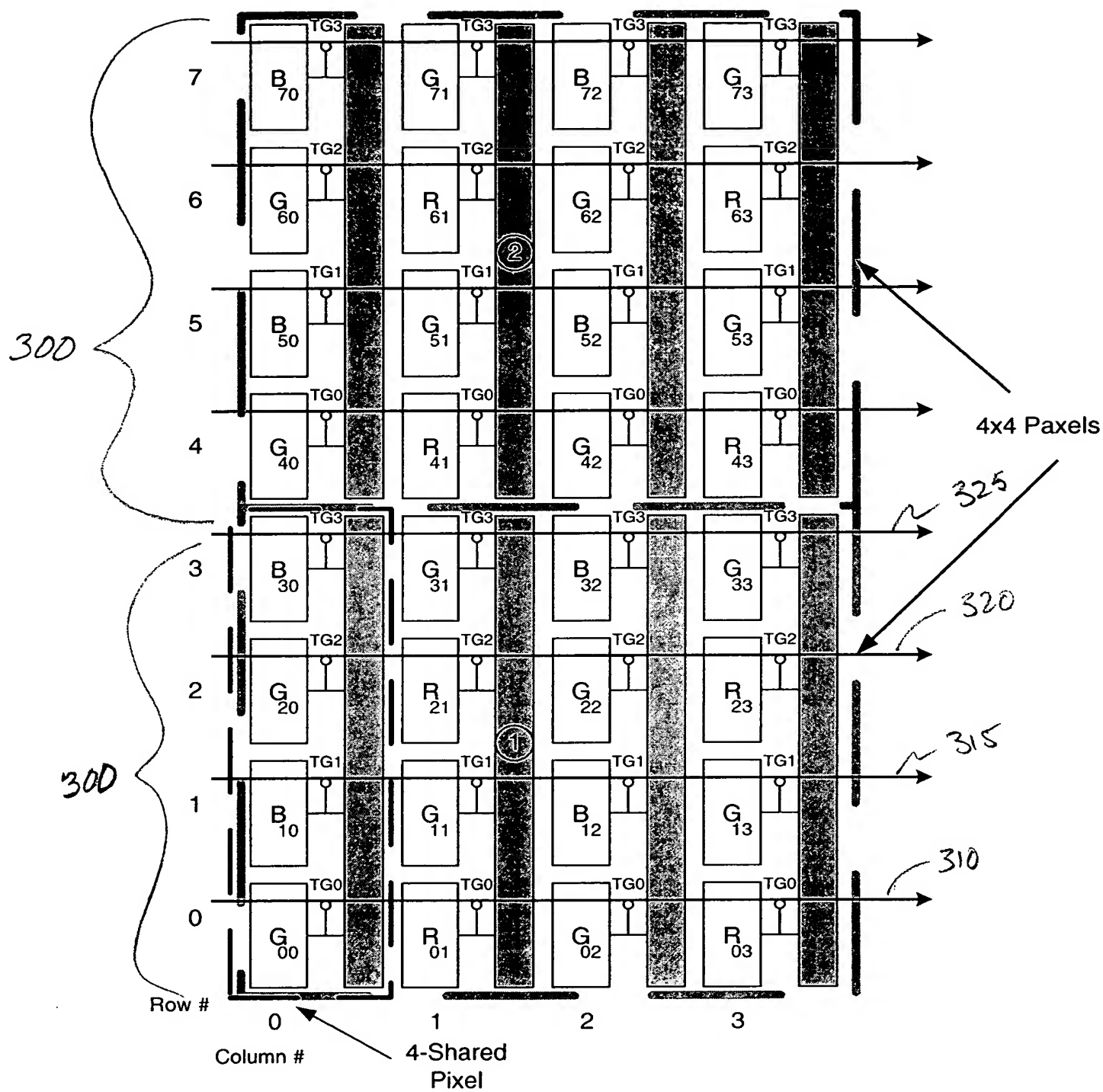


Figure 8a: 4x4 Pixel Diagram

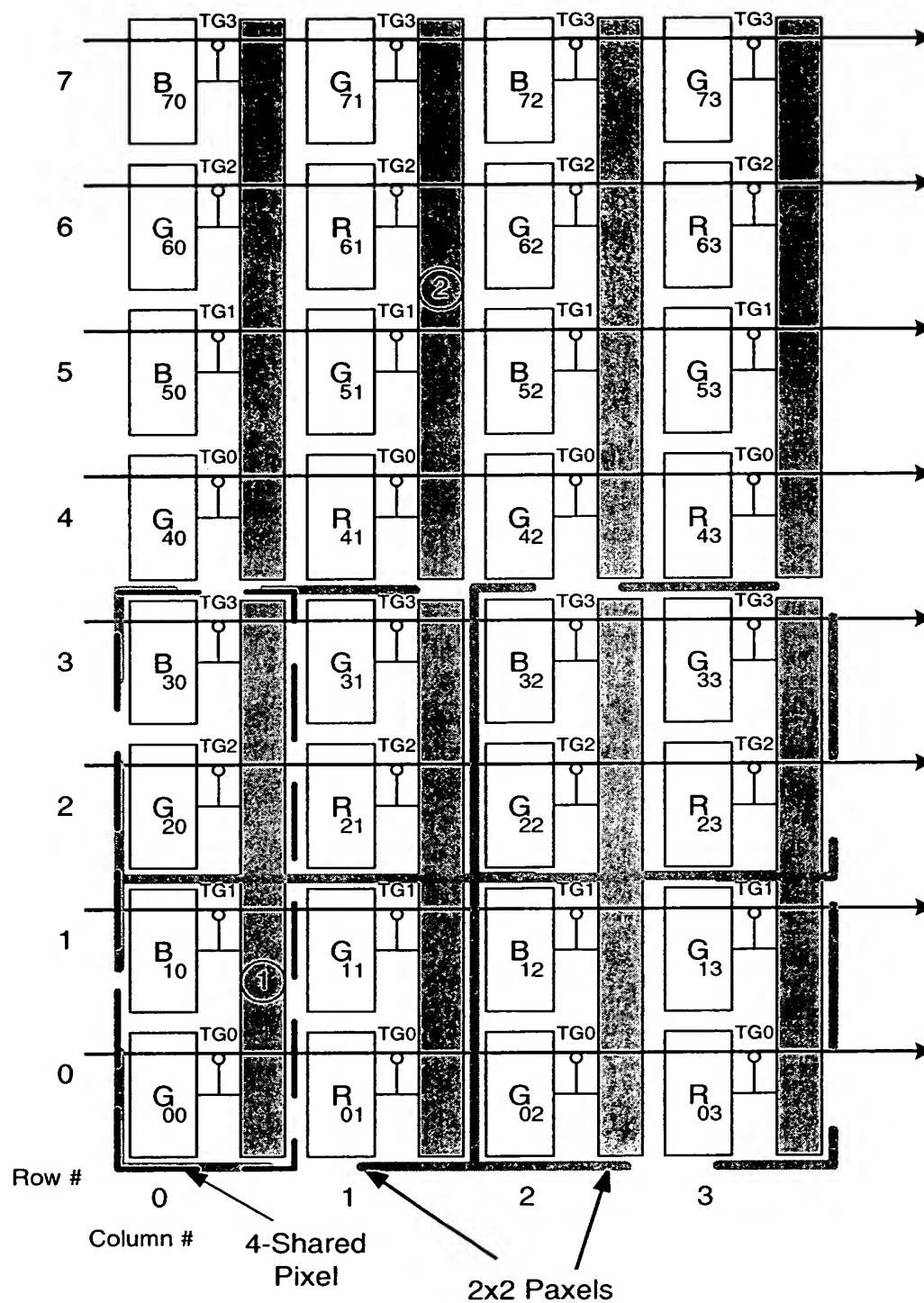


Figure 8b: 2x2 Binning and Decimation

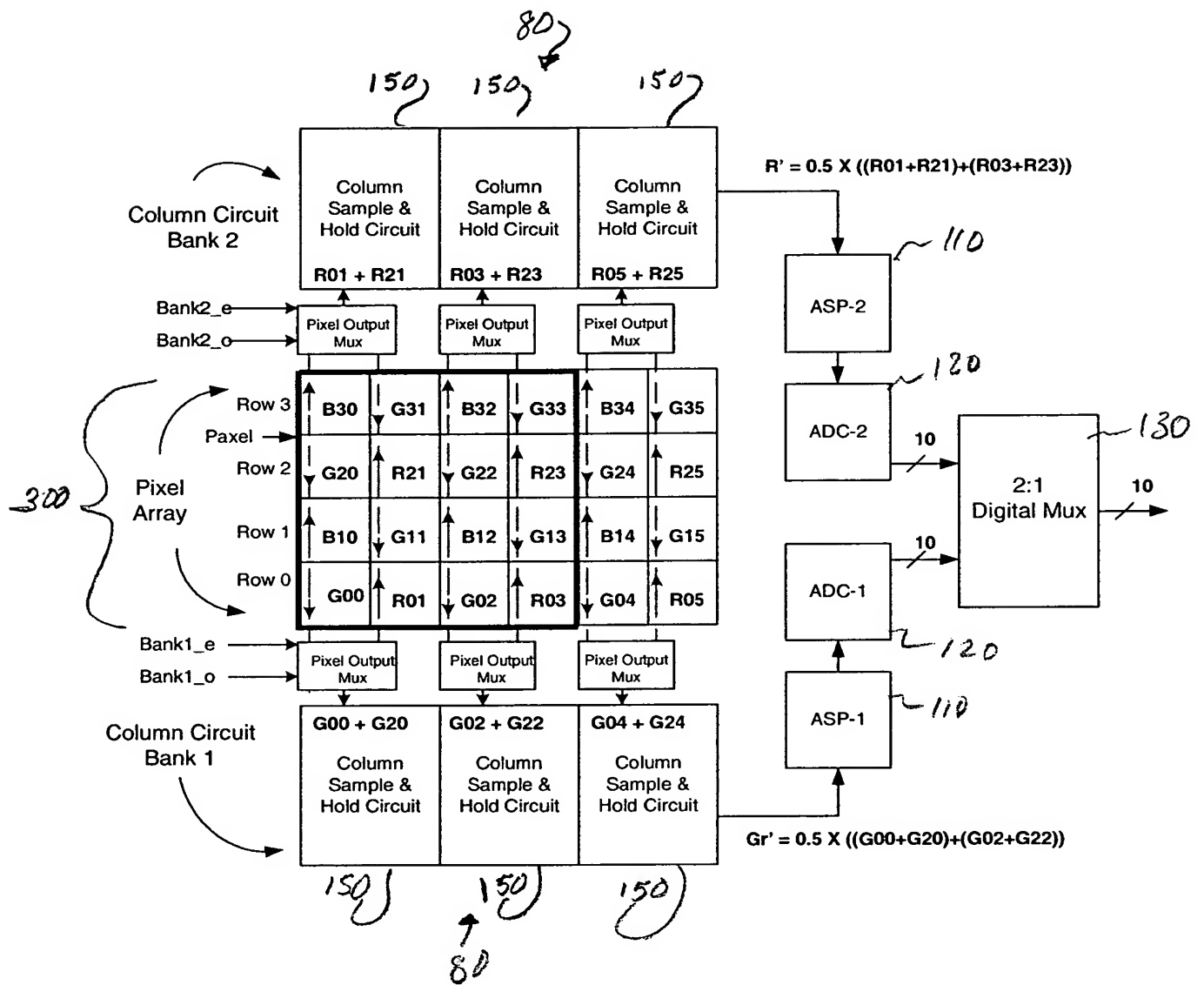


Figure 8c -

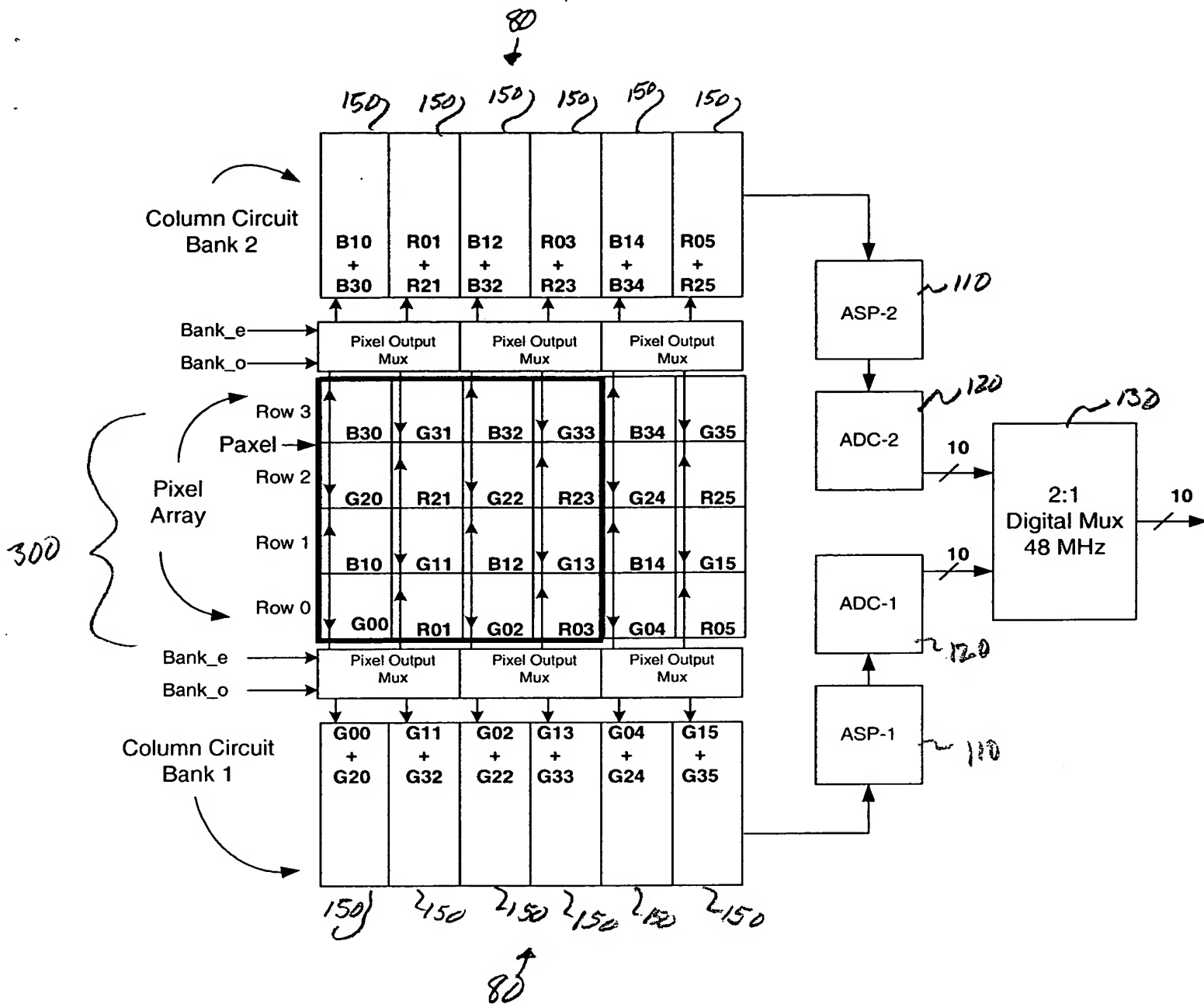


Figure 9 – Sensor Diagram for 16x Resolution Reduction

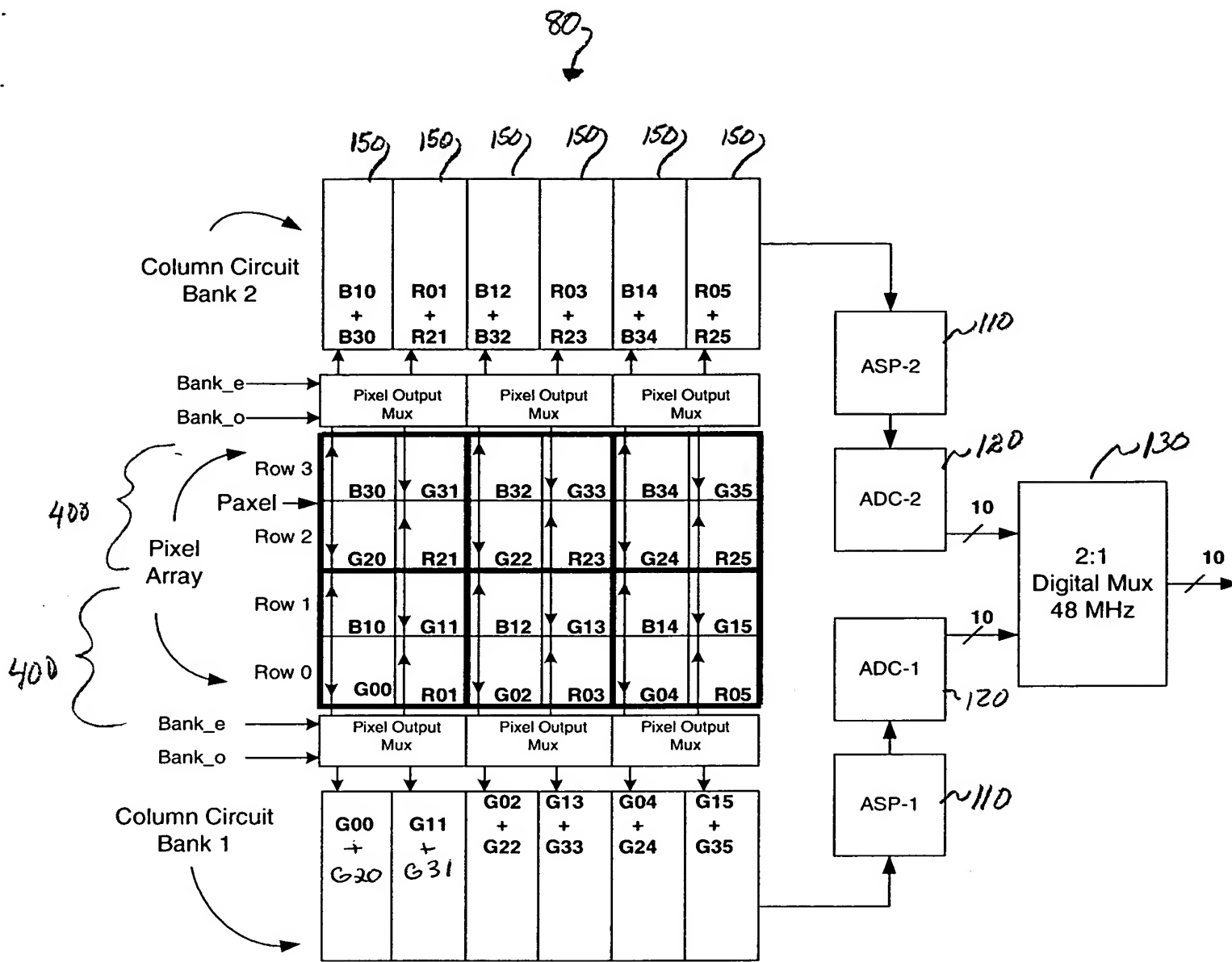


Figure 10 – Sensor Diagram for 4x Resolution Reduction

500

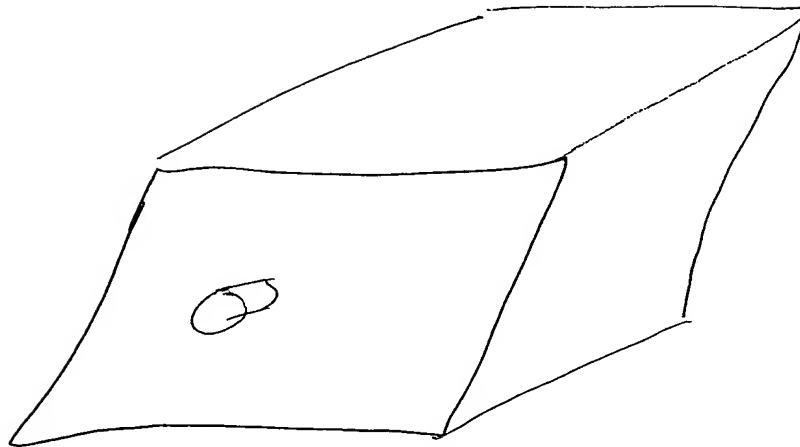


Fig. 11